NON-VOLATILE MEMORY CELLS UTILIZING SUBSTRATE TRENCHES

ABSTRACT OF THE DISCLOSURE

Several embodiments of flash EEPROM split-channel cell arrays are described that position the channels of cell select transistors along sidewalls of trenches in the substrate, thereby reducing the cell area. Select transistor gates are formed as part of the word lines and extend downward into the trenches with capacitive coupling between the trench sidewall channel portion and the select gate. In one embodiment, trenches are formed between every other floating gate along a row, the two trench sidewalls providing the select transistor channels for adjacent cells, and a common source/drain diffusion is positioned at the bottom of the trench. A third gate provides either erase or steering capabilities. In another embodiment, trenches are formed between every floating gate along a row, a source/drain diffusion extending along the bottom of the trench and upwards along one side with the opposite side of the trench being the select transistor channel for a cell. In another embodiment, select transistor gates of dual floating gate memory cells are extended into trenches or recesses in the substrate in order to lengthen the select transistor channel as the surface dimensions of the cell are being decreased. Techniques for manufacturing such flash EEPROM split-channel cell arrays are also included.